REMARKS

Claims 31, 32, and 38-54 remain pending in this application. Additionally, claims 31 and 38 have been amended/cancelled. Therefore, claims 31, 32, and 38-54 are pending in the present application.

In the Advisory Action dated March 4, 2005, the Examiner indicated that the proposed Rule 1.116 amendments provided in the Response to Final Office Action dated November 29, 2004, would not be entered. The Examiner indicated that the proposed amendments would not be entered because they raise new issued that would require additional search and consideration. Applicants respectfully assert that the amendments provided in this Preliminary Amendment indeed overcome all of the Examiner's rejections. Therefore, in light of the arguments and amendments provided in the present Preliminary Amendment, all of the claims of the present invention are allowable.

Applicants note with appreciation that in view of the Petition Decision filed on July 22, 2004, the Examiner has withdrawn all objections to the Declaration.

Applicants also note with appreciation that in view of the Amendment filed on October 12, 2004, the Examiner has withdrawn all objections to the Specification.

Applicants also acknowledge and appreciate that that in view of the Terminal Disclaimer filed on October 12, 2004, the Examiner has withdrawn all double patenting rejections.

The Examiner rejected claims 31, 32, and 38-54 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,311,299 (***Bunker***). Applicants respectfully traverse this rejection.

In light of the Amendments made to claims 31 and 38, Applicants respectfully assert that claims 31 and 38, as well as dependent claims respectively depending from claims 31 and 38 are allowable. For example, claim 31 (as amended) calls for latching a plurality of data lines, where two data lines are latched from two corresponding memory portions. Claim 31 also calls for masking the latched data lines and compressing the masked data lines using a compression circuit. Therefore, claim 31 calls for compressing latched data lines where at least two of the data lines from two different memory portions are compressed by a compressing unit. In contrast to claim 31, ***Bunker*** discloses a system where each memory array (A1-A8) corresponds with a particular data compression circuit (DC1-DC8). In other words, ***Bunker*** discloses that data from each memory array must be compressed by a separate, corresponding compression circuit. *See*, Figure 2, column 5, lines 23-35. In contrast to ***Bunker***, claim 31 recites a method that calls for a compressing circuit to compress data from at least two memory portions. Various advantages provided by the method in claim 31 is described in the specification, which includes but is not limited to, allowing a compression to be shared by a plurality of memory portion, *e.g.*, memory core, allowing for ease of re-design of memory, e.g., increasing memory density without adding additional compressing circuit. See for example, Page 12, lines 5-15 of the Specification. These advantages would not be available in the system disclosed in ***Bunker***.

The system in ***Bunker*** clearly describes that each memory portion requires a corresponding compression circuit. This disclosure does not anticipate or make obvious the

method recited in claim 31, which calls for calls for a compressing circuit to compress data from at least two memory portions. Therefore, for at least this reason, all of the elements of claim 31 is not anticipated or made obvious by ***Bunker***. Additionally, independent claim 38 calls for means for masking the latched data lines and means for compressing the masked data lines using a compression circuit. For at least the reasons cited above, claim 38 is also not anticipated by ***Bunker*** since ***Bunker*** requires that each memory portion being associated with a corresponding compressing/compression circuit. Therefore, claim 38 is also allowable for at least the reasons cited above.

There are additional reasons that support Applicants' assertions that claims 31 and 38 of the present application are allowable over ***Bunker***. For example, ***Bunker*** discloses a plurality of data masking circuits, DM1, DM2, that are coupled to particular arrays, A1 and A2. *See*, Figure 2, column 4, lines 14-19. The masking function disclosed by ***Bunker*** merely receives an array of data for each masking circuit, wherein the data lines called for by claim 31 of the present invention, where one or more of the data lines is masked based upon an enable signal. Therefore, the disclosure of ***Bunker*** does not read upon all of the elements of claim 31.

Furthermore, the function performed by the compression circuits DC1-DC8 disclosed by ***Bunker*** all receive a respective bit of read data that is applied on the data above from each of the arrays A1-A8. *See*, column 5, lines 29-31. The compression circuits DC1-DC8 makes a determination whether each of the bits applied upon its inputs has the same binary value and generates an error signal E1-E8 in response. *See,* column 5, lines 31-35. ***Bunker*** discloses that if any of the applied read data bits applied to the compensation compression circuit DC1-DC8,

has a binary value different from that of the other applied data bits, the error signal is generated. In contrast to ***Bunker***, the compression circuit called for by claim 31 of the present invention calls for detecting a predetermined pattern on a subset of data lines and to provide a pass signal when the predetermined pattern is detected on the subset of data lines. Therefore, ***Bunker*** does not disclose performing the detection of the predetermined pattern as called for by claim 1 of the present invention.

Bunker merely discloses comparing the binary value of the bits of the compensation circuit DC1-DC8 to determine whether they are equal in value, therefore, the predetermined pattern detection is not performed or disclosed by ***Bunker***. Hence, another aspect of the elements of claim 1 are not disclosed, taught, or suggested by ***Bunker***. ***Bunker*** discloses that in the masking mode, which is the mode used to read upon the claims of the present invention, when the data bit from the masking circuit is masked, the compression circuit compares the binary value of the bits from all other masking circuits and generates an error signal in response to this comparison. This is performed for individual masking circuitry and compression circuits. *See,* column 7, lines 2-6. It is clear that the system of ***Bunker*** discloses comparing binary values from other masking circuits by the compression circuit to generate an error signal. In contrast, claim 31 calls for detecting a predetermined pattern on a subset of data lines to determine whether a pass signal is to be provided based upon comparison to a predetermined pattern. This is not taught, disclosed, or suggested by ***Bunker***, which relies on comparing binary values of each bit applied to the inputs of the compression circuits DC1-DC8 to determine that an error signal is asserted. Therefore, ***Bunker*** does not disclose, teach, or suggest, all of the elements of claim 1 of the present invention.

In contrast to ***Bunker***, claim 31 calls for compressing the masked data to determine if the masked data actually matches a predetermined pattern. ***Bunker*** discloses that the test circuitry operates during a first test mode to compress test data from a plurality of memory cell arrays to generate an error signal. ***Bunker*** does not disclose compressing mask data if the mask data matches a predetermined pattern. ***Bunker*** discloses that data compression circuits include circuitry to compare each of the read data bits to see if it has a binary value different from that of other applied read data bits. However, ***Bunker*** does not disclose compressing the masked data to determine if the mask data matches a predetermined pattern.

The Examiner cites column 5, lines 54-57 in ***Bunker*** to assert that it teaches that the masked data is compressed within the compression circuit DC1-DC8 by comparing each of the applied read mask bits to a predetermined value to determine if the applied read matches the predetermined value. However, Applicants respectfully assert that column 5, lines 54-57, discloses that the data compression circuits may include circuitry to compare each of the applied read data bits to a corresponding predetermined value, which may then be used to generate an error signal. However, ***Bunker*** does not disclose compressing the mask data to determine if the mask data matches the predetermined pattern. ***Bunker*** provides data into different arrays A1-A8 into the masking circuit. In contrast, claim 31 calls for latching data present on a subset of plurality of data lines and masking the data, wherein each masking circuit is provided an array of data according to ***Bunker***, which is not taught or suggested by ***Bunker***. Furthermore, claim 31 calls for compressing the masked data to determine if the masked data matches the predetermined pattern to provide a pass signal if there is a match. ***Bunker*** does not disclose compressing the masked data to determine if the masked data matches a predetermined pattern.

Bunker merely discloses that the data compression circuit examines whether the binary value of a read bit is different from that of another read bit. Therefore, all of the elements of claim 31 are not disclosed, taught, or suggested by ***Bunker***.

Applicants respectfully also assert that the disclosure of ***Bunker*** also provides for compressing the unmasked bit to sequentially generate each error signal. *See,* for example, claim 7 of ***Bunker***. Therefore, in contrast, claim 31 calls for compressing the masked data to determine if the masked data matches the predetermined pattern. Therefore, ***Bunker*** seems to indicate the opposite of compressing the masked data, as called for by claim 31 of the present invention, since ***Bunker*** discloses compressing the unmasked bit. Accordingly, all of the elements of claim 31 are not disclosed, taught, or suggested by ***Bunker***. Additionally, claim 38 provides for a means plus function apparatus claim that calls for means for performing the similar function(s) described previously. Therefore, it is not taught, disclosed, or suggested by ***Bunker***. Therefore, claim 38 is also allowable for at least the reasons cited above.

Independent claims 31 and 38, are allowable for at least the reasons cited above. Additionally, dependent claims 32, and 39-54, which depend from independent claims 31 and 38, respectively, are also allowable for at least the reasons cited above.

The Examiner rejected claims 31, 32 and 38-54 under U.S.C. 102(f) because the Applicants did not invent the claimed subject matter in view of U.S. Patent No. 6,311,299 (***Bunker***).

As described above, independent claims 31 and 38 (both as amended) refer to compressing latched data lines where at least two of the data lines from two different memory portions are compressed by a compressing unit. These elements are not taught, disclosed, or suggested by ***Bunker***. Therefore, ***Bunker*** could not be prior art to claims of the present invention. Hence, Applicants respectfully assert that Examiner's assertion that Applicants did not invent the claimed subject matter is incorrect.

Additionally, as described above, ***Bunker*** does not disclose all of the elements of claims 31 and 38; for example, ***Bunker*** does not disclose compressing the masked data to determine if the masked data matches a predetermined pattern. Claim 31 calls for compressing the masked data to determine if the masked data matches a predetermined pattern, wherein ***Bunker*** is directed to a test circuitry that operates during a first test mode to compress test data from a plurality of memory cell arrays to generate an error signal. Further, ***Bunker*** discloses compressing an unmasked bit, wherein claims 31 and 38 call for compressing a masked bit, which is yet another example of the reasons why ***Bunker*** does not anticipate claims 31 and 38 of the present invention. Other examples of the reasons why ***Bunker*** does not disclose all of the elements of claims 31 and 38 are provided above in the previous section. Therefore, claims 31 and 38 are allowable for at least the reasons cited above.

Independent claims 31 and 38, are allowable for at least the reasons cited above. Additionally, dependent claims 32 and 38-54, which depend from independent claim 31, are also allowable for at least the reasons cited above.

Reconsideration of the present application is respectfully requested.

In light of the arguments presented above, Applicants respectfully assert that claims 31, 32, and 38-54 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the **Examiner is requested to call the undersigned attorney** at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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Date: April 29, 2005

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IN THE DRAWINGS

Applicants acknowledge that the Examiner has accepted the drawings filed on November 13, 2003.